REMARKS

Claims 1-10 are pending; claims 2-4 and 9 have been amended in several particulars.

The Examiner has indicated that "at least one full name of applicant Byoung-Han Kim is not present either in the signature or elsewhere in the papers." It is not clear exactly what the Examiner is trying to say, but it appears that the Examiner means that the inventor's signature, found on both the Declaration and Assignment, is not complete because they are signed "Kim B. H." relying on an old 1996 version of MPEP 605.04(b). The Examiner is referred to the 1998 version of the *Manual of Patent Examining Procedure*, 7th Ed. (July 1998). The Examiner is cautioned about the difference between the inventor's typewritten name and his adopted "signature". Accordingly, the objection should be withdrawn.

In paragraph 2 on page 2 of Paper No. 5, the Examiner has indicated that the Applicant is required to submit a proposed drawing correction in reply to the Office action. Note that the Examiner has not made any objections to the drawings which require such a proposed drawing correction, which are to be made in red. The Examiner then indicates that formal correction of the noted defect can be deferred and refers the Applicant to PTO FORM 948. Since the defects noted on PTO FORM 948 are matters directed to form, *i.e.,* requiring formal correction, then the requirement for correction should be deferred until the application is allowed.

Claims 2, 3, 4 and 9 have been objected to for a number of informalities noted by the Examiner. Accordingly, the foregoing amendment to the claims is believed to overcome the objection. Therefore, the objection should be withdrawn.

Claims 5 and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by Eiffel et al.. The applicant respectfully traverses this rejection for the following reason(s).

First, note that there is no reference to Eiffel et al. cited on form PTO-892, accordingly it is assumed that the Examiner is referring to U.S. Patent No. 4,654,484 to Reiffel et al. The following remarks will be based on the Reiffel et al. patent (*hereafter*: Reiffel). Second, both rejections under §102(b) set forth in Paper No. 5 based on Reiffel and applied to claims 5 and 10 are addressed herein.

Regarding claim 5, the Examiner applies Reiffel by stating, "[Reiffel teaches] analog luminance signal to parallel conversion(column 68; lines 66-68," apparently in regard to the feature of *A video signal converting apparatus which is provided to convert a first display signal of serial format into a second display signal of parallel format* set forth in the preamble of claim 5. As one of ordinary skill in the art readily knows, an "analog luminance signal" is a portion of a display signal, but is not a display signal by itself because other signals are necessary for its display. Additionally, Reifflel has no column 68, thus it is not readily apparent to the Applicant which portion of Reiffel the Examiner is relying on. Now, looking to Fig. 11 in Reiffel a color source 11

provides red, green and blue color signal to a color interface 15 for **compression and expansion** to be displayed on color display 23. Color receiving station 5 has a similar interface in order to display a color signal. Accordingly, the format of the signal output from color source 11 has the same *format* as the signal displayed by color display 23 and color receiving station 5. Therefor, Reiffel fails to disclose converting *a first display signal of serial format into a second display signal of parallel format* as required by the preamble of claim 5.

Next, the Examiner states, Reiffel teaches "means for detecting high or low signals(column 12; lines 64-68, and column 13; lines 1-8)," apparently in regard to the feature of *means for detecting a first resolution signal indicative of a resolution of said first display signal using horizontal and vertical synchronization signals related to said first display*, set forth in claim 5. Note that the "high or low signals" are described by Reiffel as timing signals of raster scan timer 166. Reiffel states, "Switch 194 and switch 196 are controlled by the raster scan timer 166. The output 210 of the raster scan timer alternates between a **high or low** signal every 63.5 microseconds. These switches 194, 196 alternately pass the output of the one line delay 198 or the output of the serial to parallel convertor 188. In the **high state**, switch 196 passes the signals on lines 190a-d. In the **low state**, switch 196 passes the signal on lines 192a-d. By alternating between these two inputs, each switch passes only one type of color difference signal, R-Y or B-Y. The digital outputs from switches 194, 196 are subsequently converted to analog R-Y and B-Y color difference signals by a red difference DAC 200 and a blue difference DAC 202. " See col. 12, line 63 through col. 13, line 8. Accordingly, the detection of high or low signals relied on by the Examiner is a detection of the state of a timer signal, not a detection of *a first resolution signal indicative of a resolution of said first display signal*

using horizontal and vertical synchronization signals related to said first display as required by claim 5. Note that the identified section of Reiffel described above and relied on by the Examiner fails to make any mention of *using horizontal and vertical synchronization signals*. In fact, it cannot be found where Reiffel discloses *using horizontal and vertical synchronization signals* anywhere in the patent.

Then, the Examiner states, Reiffel teaches "means for color difference signals(comparing signals - column 12; lines 68, and column 13; lines 1-8)," apparently in regard to the feature of *means for comparing said first resolution signal with a second resolution signal indicative of a reference resolution* set forth in claim 5. Note that the section relied on by the Examiner is provided in the preceding paragraph, and there is clearly no disclosure of a *means for comparing* and there is clearly do disclosure of a *first resolution signal* being compared to *a second resolution signal indicative of a reference resolution.*

Finally, the Examiner states, Reiffel teaches " means for converting color difference signals(converting resolution signals column 12; lines 68, and column 13; lines 1-8)," apparently in regard to the feature of *means for converting said first display signal into said second resolution signal, if there is a difference between said first and said second resolution signals* set forth in claim 5. First, Reiffel's conversion from digital color difference signals to analog color difference signals is not equivalent to *converting said first display signal into said second resolution signal.* Second, Reiffel's conversion from digital color difference signals to analog color difference signals is not is not based on whether or not *there is a difference between said first and said second resolution signals.*

Note in particular that Reiffel states, "the receiving station mirrors the sending station and produces a similar output on the receiving station color display 25." See col. 13, lines 21-23. Thus the video signal format of the sending station is the same as that of the receiving station. That is, Reiffel does not disclose converting a first display signal of serial format into a second display signal of parallel format.

Therefore, since Reiffel clearly fails to disclose all the features of claim 5, then the rejection should be withdrawn.

Regarding claim 10, the feature of *a horizontal output generator for receiving first and second data signals in response to a vertical synchronization signal and generating a horizontal output signal* is not disclosed by Reiffel. As noted above with regard to claim 5, Reiffel fails to disclose using the *vertical synchronization signal.*

The Examiner states, Reiffel teaches "video signal converting (column 11; lines 36-38, and column 12; lines 4-14), memory for storing said video signal(random access memory, column 12; lines 15-24), horizontal output generator(output of the horizontal line samples, column 11; lines 48-62), memory controller(converter, Figure 11(174), column 12; lines 1-7)."

As can be seen from the above, the Examiner fails to identify where Reiffel discloses using the *vertical synchronization signal.* See 37 CFR 1.106(b), and *Ex parte Levy*, 17 USPQ2d 1461, 1462 (1990), which states:

> "it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

Additionally, converter 174 of Fig. 11 in Reiffel is a parallel to serial converter for converting the 4 bit chrominance signal into serial data. converter 174 is clearly not *a memory controller for enabling said digital video signal to be stored in said memory.*

Also, column 11, lines 48-62, of Reiffel state, "The chrominance ADC 168 digitizes the analog output of switch 164 to four bits or 16 levels of intensity. The parallel outputs of the chrominance ADC 168 is rearranged to a serial output by the parallel to serial convertor 174. While the encoded red and blue difference signals 160, 162 are being routed to the switch 164, the luminance signal Y 158 is passed through an 8 pixel analog delay 170 and input to the luminance analog to digital convertor (ADC) 172. The luminance ADC 172 converts the intensity of each of the 640 samples contained on a horizontal line into a 5 bit value signifying 32 levels of greyscale intensity. The luminance signal Y 158 is digitized at high resolution, i.e., 640 pixels/ line, 480 lines/frame, 5 bits/pixel." The term *horizontal* is used once, in reference to "a horizontal line." Accordingly, the above noted portion of Reiffel relied on by the Examiner fails to disclose *a horizontal output generator for receiving first and second data signals in response to a vertical synchronization signal and generating a horizontal output signal, said digital video signal being in synchronization with said horizontal output signal, the pixel number per one cycle of said horizontal output signal being equal to a value of said first data signal, and the pixel number per a pulse width of said horizontal output signal being equal to a value of said second data signal*, as required by claim 10.

Accordingly, the rejection of claim 10 is deemed to be in error and should be withdrawn.

Claim 6 was rejected under 35 U.S.C. §102(b) as being anticipated by Lumelsky et al. (*hereafter*: Lumelsky). The applicant respectfully traverses this rejection for the following reason(s).

Lumelsky describes a digital television/graphics display interface for receiving digitally-encoded luminance samples and chrominance samples representing a live color television signal from a digital television decoder at a predetermined first number of television lines per frame and a second number of luminance samples per television line **and storing selected ones of the luminance samples and the chrominance samples in predetermined memory locations in a frame buffer for display in a window image in a graphics display**, the window image having a third number of rows of pixels and a fourth number of pixels per row, the third number of rows of pixels in the window image being different from the first number of television lines per frame and the fourth number of pixels per row being different from the second number of luminance samples per television line. Lumelsky fails to disclose *means for comparing the pixel number with a reference pixel number.* Here, the Examiner refers to "(television decoder and FIFO DEVICE, Figure 4(110) and Figure 5(122), column 11; lines 14-18, 22-25, 39-48, 49-66, column 21; lines 9-33)" in Lumelsky, none of which are disclosed nor disclose *means for comparing the pixel number with a reference pixel number.*

Additionally, Lumelsky fails to disclose *means for sampling said video signal using a first frequency clock generated in accordance with a difference between the pixel number and the reference pixel number* as set forth in claim 6. As noted above, there is no comparison of a pixel number to a reference pixel number, thus there can be no determination of *a difference between the*

pixel number and the reference pixel number. Here, the Examiner refers to "(column 11; lines 66-68, column 12; lines 1-22, column 13; lines 62-68, and column 14; lines 1-8)," none of which disclose *means for sampling said video signal using a first frequency clock generated* ***in accordance with a difference between the pixel number and the reference pixel number.***

The Examiner is respectfully requested, according to 37 CFR 1.106(b), to show exactly where Lumelsky discloses the comparing feature and the feature of generating a first clock frequency based on a difference between the pixel number of pixels of the video signal and the reference number.

Finally, Lumelsky fails to disclose *means for displaying said sampled video signal on said screen in synchronization with a second frequency clock generated in accordance with said difference.* As noted above there is no *difference between the pixel number and the reference pixel number* determined in Lumelsky. Although Lumelsky has means for displaying, the video signal being displayed is not displayed *in synchronization with a second frequency clock generated in accordance with said difference.* Here the Examiner refers to "(column 11; lines 15-26, and column 15; lines 35-51)." A review of Lumelsky will find disclosed therein: "The function of the image-contraction up/down counter 196 is to calculate the difference between the number of luminance samples and the number of chrominance samples written in the frame buffer 102 at any particular moment. More specifically, the image-contraction up/down counter 196 is incremented by one by each sampling-enable bit from the serial-out output 182 of the shift register 180 if the output of the chrominance pattern flip/flop 200 is zero so that chrominance sampling is disabled; the image-contraction up/down counter 196 is decremented if the output of the chrominance pattern

flip-flop 200 is one so that chrominance sampling is enabled, but luminance sampling is disabled; it is in a hold state, when luminance and chrominance data sampling are both disabled or enabled." Accordingly, the only difference determination disclosed in Lumelsky is the difference between the number of luminance samples and the number of chrominance samples written in the frame buffer 102 at any particular moment. The difference determined in Lumelsky is not equivalent to the difference determined in claim 6. Based on the difference determined in Lumelsky, it is disclosed that "If the difference between the number of luminance and chrominance samples loaded into the frame buffer 102 is more than four, and if the sampling-clock-divided-by-four signal SCK/4 from the sampling-clock divide counter 174 is in an active transition state, the upper bit of the image-contraction up/down counter 196 becomes 1 and the next sampling-clock pulse SCK loads 1 into the chrominance pattern flip/flop 200. As a result, four consecutive chrominance-shift-in pulses CFSI are issued, and four chrominance data samples are loaded into the chrominance first-in-first-out device 126 starting on a four horizontal sample boundary. When the sampling-clock-divided-by-four SCK/4 transition becomes active again after four sampling clock pulses, and the output of the image-contraction up/down counter 196 is still one, chrominance data sampling is continued. If at this moment the output of the image-contraction up/down counter 196 is zero, the chrominance-pattern flip/flop 200 becomes zero and the next four chrominance samples are skipped." Clearly, there is no disclosure of generating *a first frequency clock* in accordance with a difference between the pixel number and the reference pixel number, nor of displaying a sampled video signal on a screen in synchronization with *a second frequency clock* generated in accordance with the difference.

Accordingly, the rejection of claim 6 is deemed to be in error and should be withdrawn.

Claims 1-4 were rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over Davis in view of Reiffel. The Applicant respectfully traverses this rejection for the following reason(s).

Claim 1 calls for, a *liquid crystal display device for receiving horizontal and vertical synchronization signals and at least one analog video signal synchronized with said horizontal synchronization signal from a host and displays an image on a screen thereof.* Neither Davis nor Reiffel are directed towards a liquid crystal display device, and in fact neither one ever once mentions a liquid crystal display device. As one of ordinary skill in the art knows, the driving of and displaying of data on a liquid crystal display is quite different from the driving of and displaying of data on a cathode ray tube.

Additionally, the features of claim 1, lines 4-26 comprise the liquid crystal display, accordingly the preamble of claim 1 provides patentable weight to the claimed invention and cannot be ignored. It has long been an accepted practice in the PTO to have the preamble give meaning to the claim and properly define the invention, *Gerber Garment Technology, Inc. v. Lectra Systems, Inc.*, 916 F.2d 683, 16 USPQ 2d 1436, 1441 (Fed. Cir. 1990).

Claim 1 also calls for the liquid crystal device to comprise *a display mode discriminating means for discriminating a display mode supported by said host in response to said horizontal and vertical synchronization signals to generate first and second mode signals and first, second, third*

and fourth data signals related to said discriminated display mode. Here the Examiner relies on Davis stating:

> "Davis teaches "a system for generating high resolution video display frames from low resolution computer video output frames comprises means for storing a plurality of low horizontal and vertical resolution computer video output frames"(column 3; lines 31-36), Horizontal synch and Vertical sync signals, Red, Green, Blue, and Intensity signals(column 3; lines 36-39), 28 MHZ Clock(Figure 4 (102) and Input Sync(Figure 4(104), column 4; lines 64-68 and column 5; lines 1-20))) sync signal means, output timing circuit means(horizontal output generator, column 151 lines 47-63), control latch means(flag generator and memory selector operation, column 9; lines 5-68, and column 10; lines 1-66), and input classifier(memory operation control circuit, Figure 4(116), column 5; lines 55-68 and column 6; lines 1-2, and column 8; lines 27-30)"

According to the Examiner's statement of what Davis teaches it is not clear how the features referred to in Davis are being applied to the features of claim 1. The Examiner does not identify which of the features taught by Davis corresponds to the *display mode discriminating means.* Note that in general, the exemplary liquid crystal display device embodies a single display mode, for example, Video Graphics Array (VGA) mode, Super VGA (SVGA) mode or extended Graphics Array (XGA) mode. Davis is not related to a liquid crystal display device and does not teach discriminating any of the display modes noted above. Additionally, the *display mode discriminating means* has a function of generating *first and second mode signals and first, second, third and fourth data signals related to said discriminated display mode.* The Examiner does not indicate which of the features referred to in Davis correspond to the *first and second mode signals and first, second, third and fourth data signals* of claim 1.

Also, claim 1 calls for *a clock generator for generating first and second pixel clock signals in synchronization with said horizontal synchronization signal, said first and second pixel clock signals having frequencies corresponding to said first and second data signals, respectively, a pulse number of said first pixel clock signal corresponding to one horizontal line being equal to a value of said first data signal and a pulse number of said second pixel clock signal corresponding to one horizontal line being equal to a value of said second data signal.* Note that the Examiner referred to a 28 MHZ Clock (Figure 4 (102)) taught by Davis, however, the 28 MHZ clock signal output by clock 102 in Fig. 4 of Davis does not generate *first and second pixel clock signals in synchronization with said horizontal synchronization signal.* There has been no *prima facie* showing by the Examiner that clock 102 generates *first and second pixel clock signals in synchronization with said horizontal synchronization signal* nor has there been any showing that *said first and second pixel clock signals having frequencies corresponding to said first and second data signals, respectively.*

The Examiner also states, "Davis does not disclose analog to digital conversion means, analog to digital conversion device, random access memory with luminance signals, nor memory controlling means for analog to digital conversion." Here, the Examiner relies on the teachings found in Reiffel, stating:

> "[Reiffel teaches] an analog to digital converter(ADC) (Figure 11 (168), column 11; lines 40 -68 and column 12; lines 1- 14), random access memory with luminance access signals(Figure 10(14), column 11; lines 48-68, and column 12; lines 1- 14, column 12; lines 10- 14), and raster scanner(memory control, Figure 1 (10), column 4; lines 68 and column 5; lines 1- 18). It would have been obvious to one skilled in the art at the time of the invention to combine Davis' "Computer Video Multiplexer" with [Reiffel] et al's analog to digital conversion means because each invention share similar environments allows for

> greater retention of "...less informative bits of data ... column 2; lines 9 and 10)", which results in better resolution and a more complete picture. Furthermore, it would have been obvious for Davis and [Reiffel] et al to include the operations of memory, horizontal output generator, and memory control in a single chip because this would simplify repair of the electronic device."

The reasons of obviousness provided by the Examiner are untenable. First, one of ordinary skill in the art knows that an analog-to-digital converter does not "dispose of or "throw away" certain less informative bits of data" as suggested by the Examiner in referring to col. 2, lines 9 and 10 of Reiffel. Second, one of ordinary skill in the art knows that the disposing of or throwing away of certain less informative bits of data of a video signal results in a compressed video signal, it does not result in better resolution and a more complete picture as suggested by the Examiner. Third, the video output from the host computer in Davis is already digital and thus *an analog-to-digital converter for converting said at least one analog video signal into a digital video signal in synchronization with said first pixel clock signal* would not be required in Davis.

Further, the Examiner has not indicated why "random access memory with luminance access signals(Figure 10(14), column 11; lines 48-68, and column 12; lines 1- 14, column 12; lines 10- 14)" of Reiffel was mentioned in the Office action. That is, the Examiner has mentioned the random access memory but not explained why it was mentioned. Note that Davis teaches the computers providing a visual image output using cathode ray tubes (CRT's) "normally maintain a data representation of the image in the computer's random access memory (RAM), and periodically transmit these data to the CRT in order to produce the display image." Note further that it is the liquid crystal display device which comprises *an analog-to-digital converter for converting said at*

least one analog video signal into a digital video signal in synchronization with said first pixel clock signal, and there has been no *prima facie* showing of why it would have been obvious to one of ordinary skill in the art to include such an *analog-to-digital converter* in a liquid crystal display device based on the teachings of Davis and Reiffel, singularly, or in combination.

Likewise there has been no showing of the features of *a horizontal output generator for receiving said third and fourth data signals in response to said vertical synchronization signal and generating a horizontal output signal, said digital video signal being read from said memory in synchronization with said horizontal output signal, a pixel number per one cycle of said horizontal output signal being equal to a value of said third data signal, and a pixel number per a pulse width of said horizontal output signal being equal to a value of said fourth data signal*; and *a memory controller for enabling said digital video signal to be stored in said memory in accordance with said first and second mode signals, said horizonal synchronization signal and said first pixel clock signal, and enabling said digital video signal stored in said memory to be read from said memory in accordance with said second mode signal, said horizontal output signal and said second pixel clock signal* in the proposed combination of Davis and Reiffel.

Further, Davis discloses an apparatus for combining a plurality of low resolution, video input signals into a plurality of higher horizontal and vertical resolution video output signals whereas Reiffel discloses an apparatus for rapidly compressing, expanding, and displaying broad band information which is transmitted over a narrow band communications channel. In Davis the video is provided from a host computer to a cathode ray tube, thus there is no transmission over a narrow band communication channel. Reiffel compresses the video for transmission over a narrow band

channel, and there is no disclosure of the video being provided from a computer. It is well known in the art that computers/monitors operate in a different than televison sets and that video signals intended for display on a computer monitor are not displayable on a television set absent certain processing steps. Likewise, video intended for display on a televison set is not displayable on a computer monitor absent certain processing steps. Television signal processing and computer data processing have attained a recognized different status in the art as noted by their different classifications. Therefore, Reiffel is not analogous to Davis. Accordingly, one of ordinary skill in the art would not have looked to any teaching in Reiffel to modify Davis.

Accordingly, the rejection of claim 1 is deemed to be in error and should be withdrawn.

The Examiner has not indicated how the proposed combination of Davis and Reiffel teach any of the features set forth in claims 2 and 3. It cannot be found where either Davis or Reaiffel teach or suggest a liquid crystal display device has a memory comprising: *first, second and third memory blocks corresponding to red, green, and blue data of said digital video signal, each of said memory blocks having at least three line memories, wherein each of said line memories stores said corresponding red, green and blue data of said digital video signal from said ADC and corresponding to one horizontal line; and first, second and third multiplexers for selectively outputting data from each of said line memories of corresponding ones of said memory blocks in response to a data selection signal from said memory controller* a required by claim 2. Additionally, it cannot be found where either Davis or Reaiffel teach or suggest a liquid crystal display device has a memory controller comprising: *a flag generator for generating a plurality of write flag signals and*

a plurality of read flag signals; a memory selector for generating said first and second memory selection signals for selecting said line memories in response to said write and read flag signals to block simultaneous read and write operations of a same one of said line memories; and *a memory operation control circuit for controlling write and read access to said line mories in each of said memory blocks in response to said horizontal synchronization signal, said horizontal output signal, said first memory selection signal and said first and second pixel clock signals*, as required by claim 3. See 37 CFR 1.106(b). Accordingly, the Examiner has not provided a *prima facie* showing of obviousness. *In re Rijckaert*, 228 USPQ2d 1955 (CAFC 1993) states:

> "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rhinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976). If the examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Accordingly, the rejection of claims 2 and 3 is is deemed to be in error and should be withdrawn.

Claims 7-9 were rejected under 35 U.S.C. §103(a), as rendered obvious and unpatentable, over Lumelsky in view of Davis and Reiffel. The Applicant respectfully traverses this rejection for the following reason(s).

Claims 7-9 depend from claim 6. As noted above, Lumelsky fails to anticipate claim 6.

Neither Davis nor Reiffel provide any teachings which would have suggested that the features noted as lacking in Lumelsky with regard to claim 6 would have been obvious.

As noted with regard to claim 6, Lumelsky fails to disclose *means for sampling said video signal using a first frequency clock generated in accordance with a difference between the pixel number and the reference pixel number* as set forth in claim 6. As noted above, there is no comparison of a pixel number to a reference pixel number, thus there can be no determination of *a difference between the pixel number and the reference pixel number.* Here, the Examiner refers to "(column 11; lines 66-68, column 12; lines 1-22, column 13; lines 62-68, and column 14; lines 1-8)," none of which disclose *means for sampling said video signal using a first frequency clock generated* ***in accordance with a difference between the pixel number and the reference pixel number***. Claim 7 further limits the sampling means as comprising the features of *a first clock generator for generating said first frequency clock synchronized with said horizontal synchronization signal in response to a first data signal from said detecting means, the pulse number of said first frequency clock corresponding to one horizontal line being equal to a value of said first data signal, and a converter for converting said video signal of serial format into a video data signal of parallel format.* In the rejection of claim 7 (see Paper No. 5, paragraph 10, pages 6-7) the Examiner provides a long list of elements apparently taught by the applied references and notes that Lumelsky does not provide a teaching of any of the features of claim 7. Here the Examiner states, "Davis(U.S. Patent No. 4,851,826) teaches a first clock generator means(column 5; lines 5-20, and column 16; lines 25-33), ...horizontal line being equal to a value of said first data signal(column 5; lines 37-48), a second clock(column 16; lines 45-51), ... horizontal line being equal to a value of said

first data signal(column 5; lines 3 7-48 and column 18; lines 13-20), horizontal output generator(address generator, Figure 4(118), column 10; lines 67-68, and column 11, lines 1- 18), and converter means of sampled video signal (column 11; lines 63-68, and column 12; lines 1-14)." Note first that claim 7 does not call for "a first clock generator **means.**" Davis provides a 28 MHZ clock signal from clock 102 (col. 5, line 7). There is no teaching that clock 102 in Davis is *synchronized with said horizontal synchronization signal in response to a first data signal from said detecting means*, as required by claim 7, nor has the examiner provided a *prima facie* showing that clock 102 is *synchronized with said horizontal synchronization signal in response to a first data signal from said detecting means.* Further, claim 2 requires that *the pulse number of said first frequency clock corresponding to one horizontal line being equal to a value of said first data signal.* Since clock 102 is a 28 MHz clock and since a horizontal line has a frequency of 15.75 KHz, then it is clear that the first frequency clock does not correspond to one horizontal line. Nor does clock 102 respond to a first data signal from a detecting means. Col. 5, lines 37-48 have no relationship to clock 102, in Davis. The Examiner's statement of why it would have been obvious to combine Lumelsky and Davis is untenable and finds no basis of factual support in the teachings of either reference. Accordingly, the rejection of claim 7 is deemed to be in error and should be withdrawn.

Regarding claim 8, the Examiner refers to Davis stating, Davis teaches "a second clock(column 16; lines 45-51)." In Davis col. 16, lines 45-51 correspond to an outputting step of Davis' claim 2, which states:

"outputting each of said formed single horizontal lines at a second

clock rate substantially greater than said first clock rate thereby producing high resolution video output frames from said formed horizontal lines having a substantially higher resolution than the horizontal lines of said low resolution input frames."

There is no teaching that the "second clock rate" is synchronized with the horizontal sychronization signal. Accordingly, the rejection of claim 8 is deemed to be in error and should be withdrawn.

Claim 9 calls for *a converter for converting said sampled video signal into a data signal corresponding to the number of said horizontal lines* ***in accordance with a predetermined ratio determined by said difference between the pixel number and the reference pixel number***. Here, the Examiner has referred to Davis, (column 11; lines 63-68, and column 12; lines 1-14). In Davis, col. 11, line 63 through col. 12, line 4 state "When arbiter 162 sees RQ line 206 go low, and as soon as it deems appropriate it executes the requested data transfer cycle and then asserts an ACK on line 208. When output address generator 180 sees ACK asserted on line 208 it assumes the data transfer has been performed and unasserts signal RQ on line 206. When arbiter 162 sees RQ on 206 unasserted, it unasserts ACK on line 208. This completes the DRAM load cycle. In the time period from when RQ is asserted on line 206 and ACK is unasserted on line 208, signals XADDR on line 210 and XSEL on line 212, to be discussed hereinafter, are guaranteed to be held stable by the output address generator 180 so that the input section can perform the data transfer operation synchronously with the output address generator 180 even though both sections of the video demultiplexer are run from separate clocks. RAM arbiter 162 also observes VSD on line 148 as well as RQ to determine on a cycle by cycle basis which of three types of cycles should be run on the RAM port of frame

buffer 168. These cycles are, in order of priority, (1) writing input data to DRAMS as signaled by VSD, which indicates when input shifter 106 is full of data,"thus there does not appear to be any discussion regarding *a converter for converting said sampled video signal into a data signal corresponding to the number of said horizontal lines* nor does there appear to be any discussion of *a converter for converting said sampled video signal into a data signal corresponding to the number of said horizontal lines* ***in accordance with a predetermined ratio determined by said difference between the pixel number and the reference pixel number.*** Accordingly, the rejection of claim 9 is deemed to be in error and should be withdrawn.

The examiner is respectfully requested to reconsider the application, withdraw the objections and/or rejections and pass the application to issue in view of the above amendments and/or remarks.

Respectfully submitted,

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